



PTO/SB/088 (08-03)  
Approved for use through 07/31/2006. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE  
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>	
		Application Number	10/728,172
		Filing Date	12-03-2003
		First Named Inventor	Gattiker et al.
		Art Unit	2825
		Examiner Name	GARBOWSKI
Sheet 1	of 3	Attorney Docket Number	AUS920030654US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
WD		JONATHAN T-Y CHANG & EDWARD J. McCLUSKEY Quantitative Analysis of Very-Low-Voltage Testing, 1996	
WJ		JONATHAN T-Y CHANG, CHAO-WEN TSENG, YI-CHIN, SANJAY WATTAL, MIKE PURTELL AND EDWARD McCLUSKEY Experimental results for IDDQ and VLV Testing	
WJ		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS Circuits: Current-Voltage Signature, 1997	
WJ		R. RODRIGUIZ-MONTANES, J. FIGUERIAS IDDQ-VDD Signatures for CMOS Circuits with Bridging Defects, 1996	
WJ		R. RODRIGUIZ-MONTANES, J. FIGUERIAS Bridges in Sequential CMOS Circuits: Current-Voltage Signature, 1997	
WD		ANNE GATTIKER, PHIL NIGH, AND THOMAS VOGELS IC Testing: Background, Directions and Opportunities for Failure Analysis	
WJ		HONG HAO AND EDWARD J. McCLUSKEY "Resistive Shorts" within CMOS Gates, 1991	
WJ		HONG HAO AND EDWARD J. McCLUSKEY Very-Low-Voltage Testing for Weak CMOS Logic ICs, 1993	
WJ		HONG HAO AND EDWARD J. McCLUSKEY Analysis of Gate Oxide Shorts in CMOS Circuits, 1993	
WJ		CHARLES F. HAWKINS AND JERRY M. SODEN Electrical Failure Mode Characterization in CMOS ICs	

Examiner Signature		Date Considered	11/27/05
--------------------	--	-----------------	----------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.  
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.  
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PTO/SB/088 (08-03)  
Approved for use through 07/31/2008. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE  
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Complete if Known</b>	
		Application Number	10/728,172
		Filing Date	12-03-2003
		First Named Inventor	Gattiker et al.
		Art Unit	2825
		Examiner Name	GARGOWSKI
Sheet 2	of 3	Attorney Docket Number	AUS920030654US1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
WJ		JERRY M. SODEN, CHARLES F. HAWKINS & ANTHONY C. MILLER Identifying defects in deep-submicron CMOS ICs, 1996	
WJ		JERRY M. SODEN, CHARLES F. HAWKINS, RONALD R. FRITZEMEIER & LUTHER K. HORNING Quiescent Power Supply Current Measurement for CMOs IC Defect Detection, 1989	
WJ		DOUG JOSEPHSON, MARK STOREY, DAN DIXON, HEWLETT-PACKARD Microprocessor IDDQ Testing: A Case Study, 1995	
WJ		ALI KESHAVARZI, KAUSHIK ROY, MANOJ SACHDEV, CHARLES F. HAWKINS, K. SOUMYANATH, VLVEK DE Multiple-Parameter CMOS IC Testing with Increased Sensitivity for IDDQ, 2000	
WJ		BRAM KRUSEMAN, STEFAN van den OETELAAR, AND JOSEP RIUS Comparisons of IDDQ Testing and Very-Low Voltage Testing, 2002	
WJ		BORIS LISENER AND YURI MITNICK Fault Model for VLSI Circuits Reliability Assessment, 1999	
WJ		BORIS LISENER, DMITRY VEINGER AND YURI MITNICK Short High Voltage Stress for Design-to-Process Characterization, 1999	
WJ		PHIL NIGH AND ANNE GATTIKER Test Method Evaluation Experiments & Data, 2000	
WJ		PHIL NIGH, DAVE VALLETT, ATUL PATEL & JASON WRIGHT Failure Analysis of Timing and IDDQ-only Failures from the SEMATECH Test Methods Experiment, 1998	
WJ		ALAN W. RIGHTER, CHARLES F. HAWKINS, JERRY M. SODEN, PETER MAXWELL CMOS IC Reliability Indicators and Burn-In Economics, 1998	

Examiner Signature		Date Considered	1/27/05
--------------------	--	-----------------	---------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.  
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.  
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



PTO/SB/088 (08-03)  
Approved for use through 07/31/2006. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

## Complete if Known

Application Number	10/728,172
Filing Date	12-03-2003
First Named Inventor	Gattiker et al.
Art Unit	2825
Examiner Name	GARBOWSKI
Attorney Docket Number	AUS920030654US1

Sheet 3 of 3

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
WD		R. RODRIGUIZ-MONTANES, J.A. SEGURA, V.H. CHAMPAC, J. FIGUERAS, J.A. RUBIO Current vs. Logic Testing of Gate Oxide Short, Floating Gate and Bridging Failures in CMOS, 1991	
WD		MICHAEL RUBIN, DAVID LEARY AND SAUL NATAN Yield Enhancement and Yield Management of Silicon Foundries Using IDDQ " Stress Current Signature", 2001	
WD		YASUO SATO, MASAKI KOHNO, TOSHIO IKEDA, IWAO YAMAZAKI, & MASATO HAMAMOTO An Evaluation of Defect-Oriented Test: WELL-controlled Low Voltage Test, 2001 IEEE.	
WD		CHAO-WEN TSENG, RAY CHEN, PHIL NIGH & EDWARD J. McCLUSKEY MINVDD Testing for Weak CMOS ICs, 2001 IEEE.	
WD		T.J. VOGELS Effectiveness of I-V Testing in Comparison to IDDQ Tests, 2003 IEEE.	

Examiner Signature		Date Considered	11/2/5
--------------------	--	-----------------	--------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.